

# CS 355-01 Lab Processor Design Data Memory Debussing

Data Memory ld/sd lw/sw

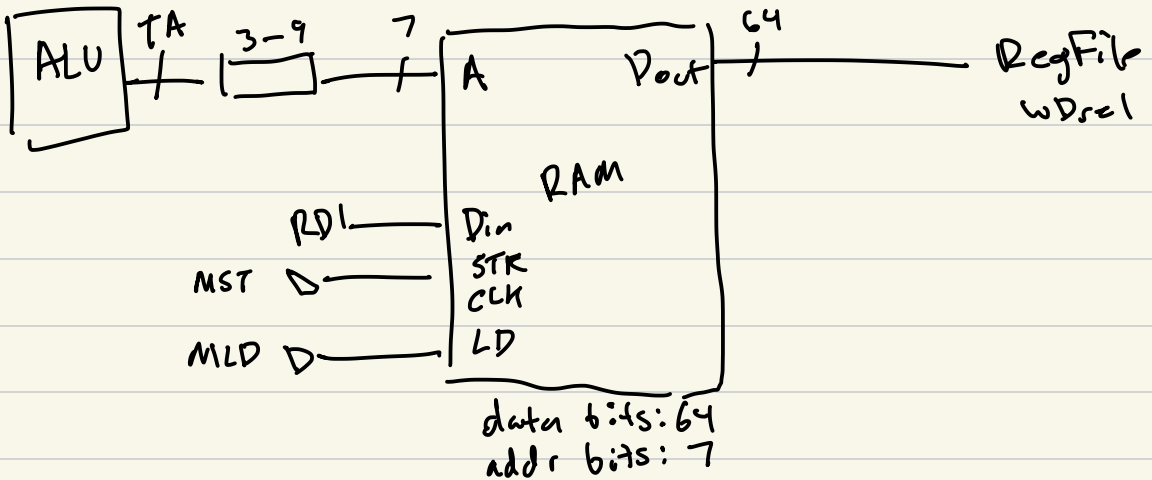
Adding a test

ASCII instruction component

Data Memory

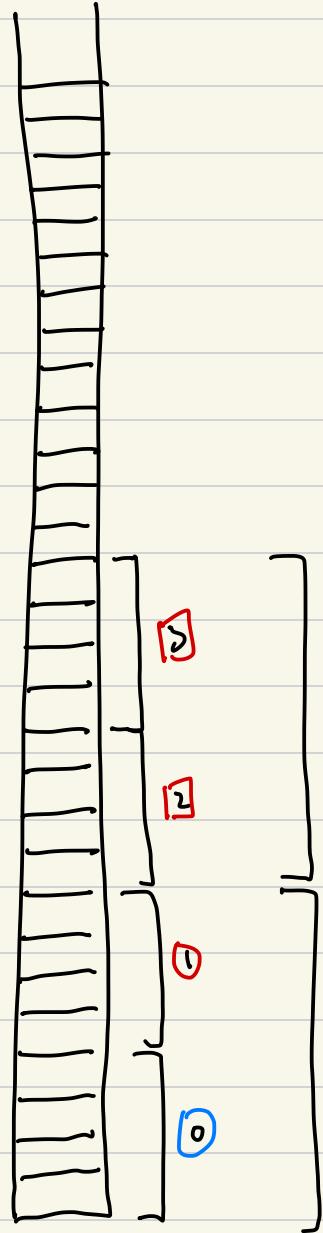
ld/sd

ld to, 16 (sp)  
└───┬───  
off + base  
sd to, 16 (sp)



1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

18  
17  
16  
15  
14  
13  
12  
11  
10  
9  
8  
7  
6  
5  
4  
3  
2  
1  
0



1

0 ←

word selector

byte

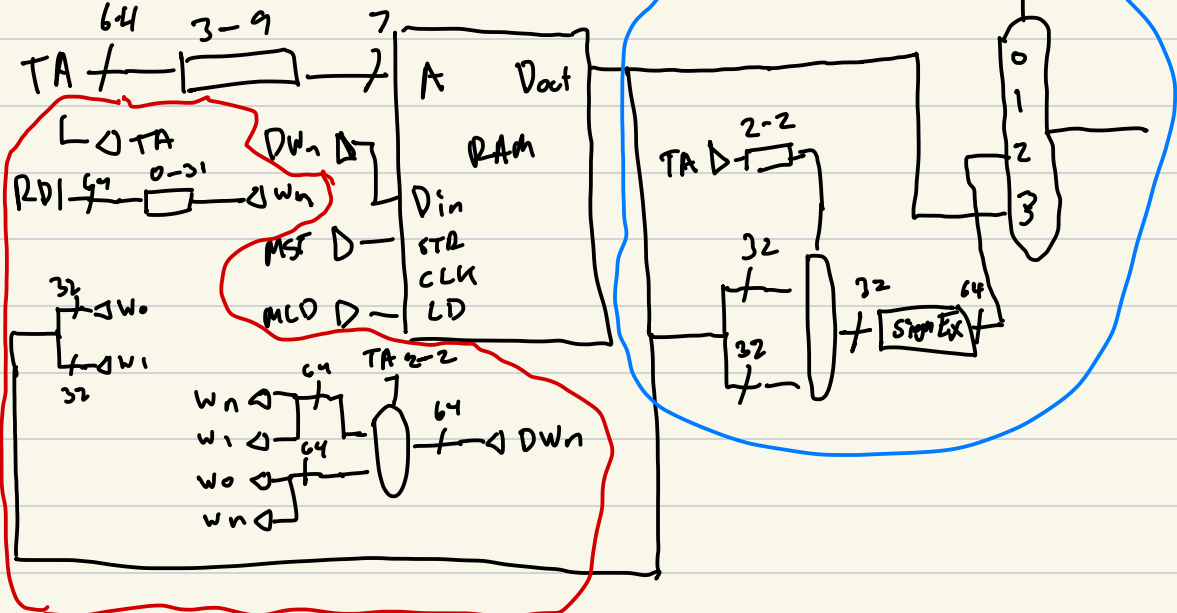
word

dword

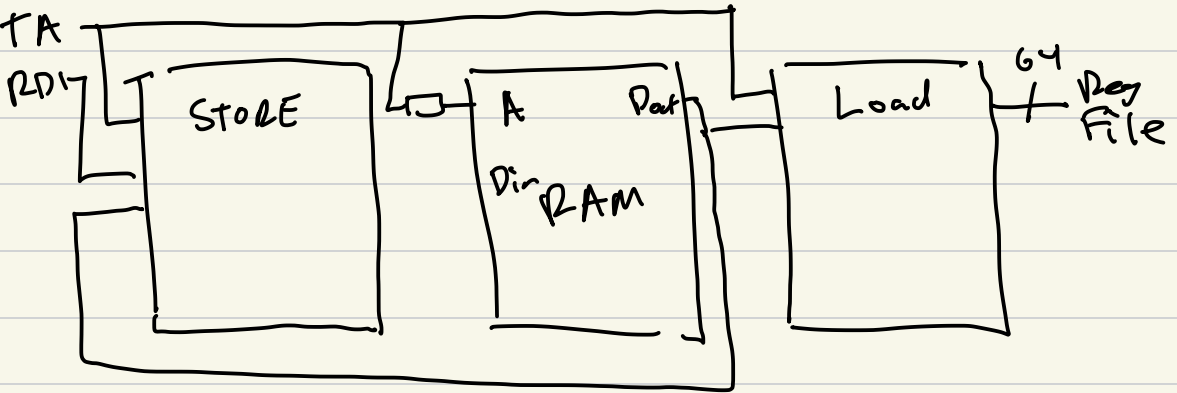
lw/sw

LOAD

- 0 byte
- 1 half
- 2 word
- 3 dword



Top level STORE



Tests

foo.s